IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

REMARKS

Objections to Claims.

The numbering of the claims has been amended to address the objections raised.

Rejection of Claims 49-56 and 59 Under 35 U.S.C. §102(b) based on *Chang* (U.S. Patent No. 4,958,321).

The invention of claim 49 is directed to a method for making a non-volatile semiconductor device. The method includes forming a multilayer gate dielectric having a charge storage layer. The multilayer gate dielectric is also dielectrically equivalent to a layer of silicon dioxide having a thickness that is less than 200 angstroms. The method further includes forming a gate comprising polycrystalline silicon of a first conductivity type on the gate dielectric. In addition, source and drain regions are formed that are separated by a channel region in a semiconductor substrate. The source and drain regions have a second conductivity type different than the first conductivity type.

As is well established, anticipation requires the presence of a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim.[1] Because the reference *Chang* does not show various limitations of claim 49, this ground for rejection is traversed.

Chang does not show a gate of a first conductivity type and source and drain regions of a different, second conductivity type. *Chang* discloses various examples of flash EPROM cells, each with a floating gate and a control gate. In all examples there is no indication of any particular type of doping for the control gates.[2] Thus, the reference does not show a gate doping of a first conductivity type that is different than a second conductivity type of a source and drain regions – and so cannot anticipate claim 49.

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[1] See Lindemann Maschinenefabrick GmbH v. American Hoist & Derrick Col., 221 USPQ 481, 485 (Fed. Cir. 1984).

[2] See *Chang*, Col. 1, Lines 47-68, which describe control gate 34 and control gate 52. There is no discussion of how or if the control gates are doped. See also Col. 7, Line 28 to Col. 8, Line 5, which describe a control gate 118 of a first embodiment, but does not indicate any kind of conductivity. Finally, see Col. 8, Lines 43-64 and Col. 9, Lines 27-20, which indicates the remaining embodiments have control gates like the first embodiment.

It is noted that *Chang* describes various approaches to doping a floating gate. However such teachings also fail to show all limitations of claim 49. First, while doped floating gates are shown, no particular conductivity type for the doping is disclosed. Second, if a floating gate is construed as gate according to claim 49, then the reference does not show a multilayer gate dielectric with charge storing layer.

As noted above, claim 49 recites a method that forms a gate of a first conductivity type that is different then second conductivity type source and drain regions. In *Chang*, no particular conductivity type for floating gates is shown.[3]

Claim 49 also recites forming the gate over a gate dielectric, where the gate dielectric is a multilayered gate dielectric with a charge storing layer. Such a limitation is not shown in *Chang*.

In *Chang* floating gates are formed over a single layer dielectric, not multilayered dielectrics, and such single layer dielectrics do not include a charge storing layer.[4]

Claim 53, which depends from claim 49, includes additional limitations not shown in *Chang*. Claim 53 recites that forming a charge storing layer includes forming a layer selected form the group consisting or silicon nitride, silicon oxynitride, silicon-rich silicon dioxide, and a ferroelectric material.

Chang shows the formation of gate dielectrics, tunnel dielectrics and intergate dielectrics. Such dielectrics are described as being formed from silicon dioxide or silicon nitride. However, none of these structures in *Chang* is described as a charge storing layer.[5] The only charge storing structure disclosed in *Chang* is a floating gate of polysilicon, which is clearly outside the list of materials set forth in claim 53.

For all of these reasons, the rejection of claims 49-56 and 59 is traversed.

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[3] See *Chang*, Col. 1, Line 47 to Col. 2, Line 11, which describe floating gates 30 and 48, without any discussion of conductivity type. See also, Col. 7, Line 1 to 27, which describes doping levels for a floating gate, but never disclose conductivity type (e.g., an n- or p-type dopant).

[4] See *Chang*, Col. 1, Lines 55-56 and FIGS. 1 and 2, which show floating gates (30 and 48) over tunnel oxide 28 and gate oxide 46. However, the floating gates are never described as being formed over a multilayered or charge storing dielectric. Similarly, Col. 6, Lines 13-58, which describes a multi-thickness dielectric layer that is never indicated as including a charge storing layer.

[5] See *Chang*, all examples. Tunnel dielectrics, gate dielectrics and integrate dielectrics are never described as charge storing layers.

Rejection of Claims 57-59 Under 35 U.S.C. §103(a), based on *Chang* in view of *Vinal* (U.S. Patent 4,990,974).

As is well known, to establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.

It is not believed a prima facie case of obviousness has been established as motivation is lacking for the proposed combination of *Chang* in view of *Vinal*.

Vinal appears to teach away from the modification relied upon in the rejection. *Vinal* is directed toward the formation of a "Fermi-FET." *Vinal* describes an approach to compensating for a flatband voltage arising from ohmic metal contacts. In such an approach, a polysilicon gate is doped to match a substrate doping.[6] However, while such an approach may be effective to Fermi-FET device, *Vinal* indicates that such an approach for a standard (i.e., non-Fermi) FET results in undesirable effects.[7] Thus, modifying *Chang* according to *Vinal* would result in a device that suffers from the indicated drawbacks.

Because the cited reference *Vinal* teaches away from the modification relied upon in the rejection, it is believed motivation for the combination is lacking. Accordingly, a prima facie case of obviousness has not been established, and this ground for rejection is traversed.

Rejection of Claims 60-69 Under 35 U.S.C. §102(b) based on *Lancaster et al.* (U.S. Patent No. 4,958,321).

The invention of claim 60 includes a method with the steps of applying an electric field to a charge storing layer in a multilayer dielectric. The multilayer dielectric is disposed between a first semiconductor layer and a second semiconductor layer. The method also includes applying the electric field to form a charge accumulation region in the first semiconductor layer proximate to the multilayer gate dielectric and a charge depletion region in the second semiconductor layer proximate to the multilayer gate dielectric.

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[6] See *Vinal*, Col. 21, Line 60-66, and FIG. 10B.

[7] See *Vinal*, Col. 25, Lines 30-49, which indicates a conventional FET either suffers from undesirable punch-through voltages, or requires high doping that can require channel surface compensation.

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As previously noted, anticipation requires the presence of a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim.

Applicant's claim 60 recites forming, by application of an electric field, a charge accumulation region proximate to multilayer gate dielectric and forming a charge depletion region proximate to the multilayer gate dielectric. Such limitations are not shown in the cited reference. The rejection cites the presence of a charge accumulation layer and depletion layers in *Lancaster*. However, the rejection provides no indication as to the proximity of the layer with respect to a multilayer gate dielectric. Consequently, the rejection does not establish a case of anticipation as every element of claim 60 has not been shown to be arranged as in the claim.

For this reason, the rejection of claims 60-69 is traversed.

Claims 49 and 65-68 have been amended to address typographical errors and not in response to the cited art. The present claims 49-69 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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Version With Markings to Show Changes Made

In the Claims.

49. (Twice Amended) A method for making a non-volatile semiconductor device comprising:

forming a multilayer gate dielectric having a charge storage layer and being dielectrically equivalent to a layer of silicon dioxide having a thickness that is less than 200 angstroms;

forming a gate comprising polycrystalline silicon of a first conductivity type on said gate dielectric; and

forming source and drain regions separated by a channel region in a semiconductor substrate, said source and drain regions having a second conductivity type different from said first conductivity type.

66 [65]. (Amended) The method of claim 64, wherein:

the charge storage layer comprises silicon nitride.

67 [66]. (Amended) The method of claim 60, wherein:

the first semiconductor layer comprises a p-type gate; and

the second semiconductor layer comprises a p-type channel disposed between n-type source/drain regions.

68 [67]. (New) The method of claim 60, wherein:

the first semiconductor layer comprises an n-type gate; and

the second semiconductor layer comprises an n-type channel disposed between p-type source/drain regions.

69 [68]. (New) The method of claim 60, wherein:

the multilayer gate dielectric comprises a charge storage layer selected from the group consisting of silicon nitride, silicon oxynitride, silicon-rich silicon dioxide, and a ferroelectric material.